

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 instruction tests for VRR-c encoded:
				5 *
				6 * E785 VBPERM - Vector Bit Permute
				7 *
				8 * James Wekel March 2025
				9 *****
				11 *****
				12 *
				13 * basic instruction tests
				14 *
				15 *****
				16 * This program tests proper functioning of the z/arch E7 VRR-c
				17 * Vector Bit Permute instruction.
				18 *
				19 * Exceptions are not tested.
				20 *
				21 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				22 * obvious coding errors. None of the tests are thorough. They are
				23 * NOT designed to test all aspects of any of the instructions.
				24 *
				25 *****
				26 *
				27 * *Testcase zvector-e7-18-VBPERM
				28 * *
				29 * * Zvector E7 instruction tests for VRR-c encoded:
				30 * *
				31 * * E785 VBPERM - Vector Bit Permute
				32 * *
				33 * * # -----
				34 * * # This tests only the basic function of the instructions.
				35 * * # Exceptions are NOT tested.
				36 * * # -----
				37 * *
				38 * main size 2
				39 * numcpu 1
				40 * sysclear
				41 * archlvl z/Arch
				42 *
				43 * loadcore "\$(testpath)/zvector-e7-18-VBPERM core" 0x0
				44 *
				45 * diag8cmd enable # (needed for messages to Hercules console)
				46 * runtest 5
				47 * diag8cmd disable # (reset back to default)
				48 *
				49 * *Done
				50 *
				51 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				53 *****
				54 * FCHECK Macro - Is a Facility Bit set?
				55 *
				56 * If the facility bit is NOT set, an message is issued and
				57 * the test is skipped.
				58 *
				59 * Fcheck uses R0, R1 and R2
				60 *
				61 * eg. FCHECK 134, 'vector-packed-decimal'
				62 *****
				63 MACRO
				64 FCHECK &BITNO, &NOTSETMSG
				65 . * &BITNO : facility bit number to check
				66 . * &NOTSETMSG : 'facility name'
				67 LCLA &FBBYTE Facility bit in Byte
				68 LCLA &FBBIT Facility bit within Byte
				69
				70 LCLA &L(8)
				71 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				72
				73 &FBBYTE SETA &BITNO/8
				74 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				75 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				76
				77 B X&SYSNDX
				78 * Fcheck data area
				79 * skip messgae
				80 SKT&SYSNDX DC C' Skipping tests: '
				81 DC C&NOTSETMSG
				82 DC C' (bit &BITNO) is not installed.'
				83 SKL&SYSNDX EQU *-SKT&SYSNDX
				84 * facility bits
				85 DS FD gap
				86 FB&SYSNDX DS 4FD
				87 DS FD gap
				88 *
				89 X&SYSNDX EQU *
				90 LA R0, ((X&SYSNDX-FB&SYSNDX)/8)-1
				91 STFLE FB&SYSNDX get facility bits
				92
				93 XGR R0, R0
				94 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				95 N R0, =F' &FBBIT' is bit set?
				96 BNZ XC&SYSNDX
				97 *
				98 * facility bit not set, issue message and exit
				99 *
				100 LA R0, SKL&SYSNDX message length
				101 LA R1, SKT&SYSNDX message address
				102 BAL R2, MSG
				103
				104 B EOJ
				105 XC&SYSNDX EQU *
				106 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				108	*****		
				109	* Low core PSWs		
				110	*****		
00000000		00000000	0000163B	111	ZVE7TST START 0		
		00000000		112	USING ZVE7TST, R0	Low core addressability	
		00000140	00000000	113			
				114	SVOLDPSW EQU ZVE7TST+X' 140'	z/Arch Supervisor call old PSW	
00000000		00000000	000001A0	116	ORG ZVE7TST+X' 1A0'	z/Architecture RESTART PSW	
000001A0	00000001 80000000			117	DC X' 0000000180000000'		
000001A8	00000000 00000200			118	DC AD(BEGIN)		
000001B0		000001B0	000001D0	120	ORG ZVE7TST+X' 1D0'	z/Architecture PROGRAM CHECK PSW	
000001D0	00020001 80000000			121	DC X' 0002000180000000'		
000001D8	00000000 0000DEAD			122	DC AD(X' DEAD')		
000001E0		000001E0	00000200	124	ORG ZVE7TST+X' 200'	Start of actual test program..	
				126	*****		
				127	* The actual "ZVE7TST" program itself...		
				128	*****		
				129	* Architecture Mode: z/Arch		
				130	* Register Usage:		
				131	* R0 (work)		
				132	* R1-4 (work)		
				133	* R5 Testing control table - current test base		
				134	* R6- R7 (work)		
				135	* R8 First base register		
				136	* R9 Second base register		
				137	* R10 Third base register		
				138	* R11 E7TEST call return		
				139	* R12 E7TESTS register		
				140	* R13 (work)		
				141	* R14 Subroutine call		
				142	* R15 Secondary Subroutine call or work		
				143	* *****		
				144	*****		
00000200		00000200		148	USING BEGIN, R8	FIRST Base Register	
00000200		00001200		149	USING BEGIN+4096, R9	SECOND Base Register	
00000200		00002200		150	USING BEGIN+8192, R10	THIRD Base Register	
00000200	0580			152	BEGIN BALR R8, 0	Inititalize FIRST base register	
00000202	0680			153	BCTR R8, 0	Inititalize FIRST base register	
00000204	0680			154	BCTR R8, 0	Inititalize FIRST base register	
00000206	4190 8800		00000800	156	LA R9, 2048(, R8)	Inititalize SECOND base register	
0000020A	4190 9800		00000800	157	LA R9, 2048(, R9)	Inititalize SECOND base register	
				158			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000020E	41A0 9800		00000800	159	LA	R10, 2048(, R9)	Initialize THIRD base register
00000212	41A0 A800		00000800	160	LA	R10, 2048(, R10)	Initialize THIRD base register
				161			
00000216	B600 8324		00000524	162	STCTL	R0, R0, CTLR0	Store CR0 to enable AFP
0000021A	9604 8325		00000525	163	OI	CTLR0+1, X' 04'	Turn on AFP bit
0000021E	9602 8325		00000525	164	OI	CTLR0+1, X' 02'	Turn on Vector bit
00000222	B700 8324		00000524	165	LCTL	R0, R0, CTLR0	Reload updated CR0
				166			
				167	*****		
				168	* Is z/Architecture vector facility installed (bit 129)		
				169	* Is z/Architecture vector enhancements facility 1 installed (bit 135)		
				170	*****		
00000226	47F0 80A8		000002A8	171	FCHECK	129, 'z/Architecture vector facility'	
				172+	B	X0001	
				173+*			Fcheck data area
				174+*			skip messgae
0000022A	40404040 E2928997			175+SKT0001	DC	C'	Skipping tests: '
0000023E	A961C199 838889A3			176+	DC	C' z/Architecture vector facility'	
0000025C	404D8289 A340F1F2			177+	DC	C' (bit 129) is not installed.'	
		0000004E	00000001	178+SKL0001	EQU	*- SKT0001	
				179+*			facility bits
00000278	00000000 00000000			180+	DS	FD	gap
00000280	00000000 00000000			181+FB0001	DS	4FD	
000002A0	00000000 00000000			182+	DS	FD	gap
				183+*			
		000002A8	00000001	184+X0001	EQU	*	
000002A8	4100 0004		00000004	185+	LA	R0, ((X0001- FB0001)/8) - 1	
000002AC	B2B0 8080		00000280	186+	STFLE	FB0001	get facility bits
000002B0	B982 0000			187+	XGR	R0, R0	
000002B4	4300 8090		00000290	188+	IC	R0, FB0001+16	get fbit byte
000002B8	5400 832C		0000052C	189+	N	R0, =F' 64'	is bit set?
000002BC	4770 80D0		000002D0	190+	BNZ	XC0001	
				191+*			
				192+*	facility bit not set, issue message and exit		
				193+*			
000002C0	4100 004E		0000004E	194+	LA	R0, SKL0001	message length
000002C4	4110 802A		0000022A	195+	LA	R1, SKT0001	message address
000002C8	4520 8240		00000440	196+	BAL	R2, MSG	
000002CC	47F0 8308		00000508	197+	B	E0J	
		000002D0	00000001	198+XC0001	EQU	*	
				199	FCHECK	135, 'z/Arch vector enhance facility 1'	
000002D0	47F0 8158		00000358	200+	B	X0002	
				201+*			Fcheck data area
				202+*			skip messgae
000002D4	40404040 E2928997			203+SKT0002	DC	C'	Skipping tests: '
000002E8	A961C199 838840A5			204+	DC	C' z/Arch vector enhance facility 1'	
00000308	404D8289 A340F1F3			205+	DC	C' (bit 135) is not installed.'	
		00000050	00000001	206+SKL0002	EQU	*- SKT0002	
				207+*			facility bits
00000328	00000000 00000000			208+	DS	FD	gap
00000330	00000000 00000000			209+FB0002	DS	4FD	
00000350	00000000 00000000			210+	DS	FD	gap
				211+*			
		00000358	00000001	212+X0002	EQU	*	
00000358	4100 0004		00000004	213+	LA	R0, ((X0002- FB0002)/8) - 1	
0000035C	B2B0 8130		00000330	214+	STFLE	FB0002	get facility bits

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				353 *****
				354 * Normal completion or Abnormal termination PSWs
				355 *****
000004F8	00020001 80000000			357 E0JPSW DC 0D' 0' , X' 0002000180000000' , AD(0)
00000508	B2B2 82F8		000004F8	359 E0J LPSWE E0JPSW Normal completion
00000510	00020001 80000000			361 FAILPSW DC 0D' 0' , X' 0002000180000000' , AD(X' BAD')
00000520	B2B2 8310		00000510	363 FAILTEST LPSWE FAILPSW Abnormal termination
				365 *****
				366 * Working Storage
				367 *****
00000524	00000000			369 CTLR0 DS F CRO
00000528	00000000			370 DS F
0000052C				372 LTORG , Literals pool
0000052C	00000040			373 =F' 64'
00000530	00000001			374 =F' 1'
00000534	00001608			375 =A(E7TESTS)
00000538	0000			376 =H' 0'
0000053A	005F			377 =AL2(L' MSGMSG)
				378
				379 * some constants
				380
	00000400	00000001		381 K EQU 1024 One KB
	00001000	00000001		382 PAGE EQU (4*K) Size of one page
	00010000	00000001		383 K64 EQU (64*K) 64 KB
	00100000	00000001		384 MB EQU (K*K) 1 MB
				385
	AABBCCDD	00000001		386 REG2PATT EQU X' AABBCCDD' Polluted Register pattern
	000000DD	00000001		387 REG2LOW EQU X' DD' (last byte above)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				427	*****
				428	* E7TEST DSECT
				429	*****
				431	E7TEST DSECT ,
00000000	00000000			432	TSUB DC A(0) pointer to test
00000004	0000			433	TNUM DC H' 00' Test Number
00000006	00			434	DC X' 00'
00000007	00			435	DC HL1' 00' m field - not used
				436	
00000008	40404040	40404040		437	OPNAME DC CL8' ' E7 name
00000010	00000000			438	V2ADDR DC A(0) address of v2 source
00000014	00000000			439	V3ADDR DC A(0) address of v3 source
00000018	00000000			440	RELEN DC A(0) RESULT LENGTH
0000001C	00000000			441	READRR DC A(0) result (expected) address
00000020	00000000	00000000		442	DS FD gap
00000028	00000000	00000000		443	V10OUTPUT DS XL16 V1 Output
00000038	00000000	00000000		444	DS FD gap
				445	
				446	* test routine will be here (from VRR-c macro)
				447	*
				448	* followed by
				449	* EXPECTED RESULT
				451	ZVE7TST CSECT ,
000010A8		00000000	0000163B	452	DS 0F
				454	*****
				455	* Macros to help build test tables
				456	*****
				458	*
				459	* macro to generate individual test
				460	*
				461	MACRO
				462	VRR_C &INST
				463	. * &INST - VRR-c instruction under test
				464	. * no m fields
				465	
				466	GBLA &TNUM
				467	&TNUM SETA &TNUM+1
				468	
				469	DS 0FD
				470	USING *, R5 base for test data and test routine
				471	
				472	T&TNUM DC A(X&TNUM) address of test routine
				473	DC H' &TNUM test number
				474	DC X' 00'
				475	DC HL1' 00' m field
				476	DC CL8' &INST' instruction name
				477	DC A(RE&TNUM+16) address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				526	*****
				527	* E7 VRR-c tests
				528	*****
				529	PRINT DATA
				530	*
				531	* E785 VBPERM - Vector Bit Permute
				532	*
				533	* VRR-c instruction
				534	* followed by
				535	* 16 byte expected result (V1)
				536	* 16 byte V2 source
				537	* 16 byte V3 source
				538	*-----
				539	* VBPERM - Vector Bit Permute
				540	*-----
				541	
				542	VRR_C VBPERM
000010A8				543+	DS OFD
000010A8		000010A8		544+	USING *, R5
000010A8	000010E8			545+T1	DC A(X1)
000010AC	0001			546+	DC H' 1'
000010AE	00			547+	DC X' 00'
000010AF	00			548+	DC HL1' 00'
000010B0	E5C2D7C5 D9D44040			549+	DC CL8' VBPERM
000010B8	00001120			550+	DC A(RE1+16)
000010BC	00001130			551+	DC A(RE1+32)
000010C0	00000010			552+	DC A(16)
000010C4	00001110			553+REA1	DC A(RE1)
000010C8	00000000 00000000			554+	DS FD
000010D0	00000000 00000000			555+V101	DS XL16
000010D8	00000000 00000000				
000010E0	00000000 00000000			556+	DS FD
				557+*	
000010E8				558+X1	DS OF
000010E8	E310 5010 0014		00000010	559+	LGF R1, V2ADDR
000010EE	E761 0000 0806		00000000	560+	VL v22, 0(R1)
000010F4	E310 5014 0014		00000014	561+	LGF R1, V3ADDR
000010FA	E771 0000 0806		00000000	562+	VL v23, 0(R1)
00001100	E766 7000 0E85			563+	VBPERM V22, V22, V23
00001106	E760 5028 080E		000010D0	564+	VST V22, V101
0000110C	07FB			565+	BR R11
00001110				566+RE1	DC OF
00001110				567+	DROP R5
00001110	00000000 00000000			568	DC XL16' 0000000000000000 0000000000000000'
00001118	00000000 00000000				
00001120	00000000 00000000			569	DC XL16' 0000000000000000 0000000000000000'
00001128	00000000 00000000				
00001130	00000000 00000000			570	DC XL16' 0000000000000000 0000000000000000'
00001138	00000000 00000000				
				571	
				572	VRR_C VBPERM
00001140				573+	DS OFD
00001140		00001140		574+	USING *, R5
00001140	00001180			575+T2	DC A(X2)
00001144	0002			576+	DC H' 2'
00001146	00			577+	DC X' 00'

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001147	00			578+	DC	HL1' 00'	m field
00001148	E5C2D7C5 D9D44040			579+	DC	CL8' VBPERM	instruction name
00001150	000011B8			580+	DC	A(RE2+16)	address of v2 source
00001154	000011C8			581+	DC	A(RE2+32)	address of v3 source
00001158	00000010			582+	DC	A(16)	result length
0000115C	000011A8			583+REA2	DC	A(RE2)	result address
00001160	00000000 00000000			584+	DS	FD	gap
00001168	00000000 00000000			585+V102	DS	XL16	V1 output
00001170	00000000 00000000						
00001178	00000000 00000000			586+	DS	FD	gap
				587+*			
00001180				588+X2	DS	0F	
00001180	E310 5010 0014		00000010	589+	LGF	R1, V2ADDR	load v2 source
00001186	E761 0000 0806		00000000	590+	VL	v22, 0(R1)	use v22 to test decoder
0000118C	E310 5014 0014		00000014	591+	LGF	R1, V3ADDR	load v3 source
00001192	E771 0000 0806		00000000	592+	VL	v23, 0(R1)	use v23 to test decoder
00001198	E766 7000 0E85			593+	VBPERM	V22, V22, V23	test instruction (dest is a source)
0000119E	E760 5028 080E		00001168	594+	VST	V22, V102	save v1 output
000011A4	07FB			595+	BR	R11	return
000011A8				596+RE2	DC	0F	xl16 expected result
000011A8				597+	DROP	R5	
000011A8	00000000 00000000			598	DC	XL16' 0000000000000000 0000000000000000'	result t
000011B0	00000000 00000000						
000011B8	FFFFFFFF FFFFFFFF			599	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
000011C0	FFFFFFFF FFFFFFFF						
000011C8	FFFFFFFF FFFFFFFF			600	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
000011D0	FFFFFFFF FFFFFFFF						
				601			
				602	VRR_C	VBPERM	
000011D8				603+	DS	0FD	
000011D8		000011D8		604+	USING	*, R5	base for test data and test routine
000011D8	00001218			605+T3	DC	A(X3)	address of test routine
000011DC	0003			606+	DC	H' 3'	test number
000011DE	00			607+	DC	X' 00'	
000011DF	00			608+	DC	HL1' 00'	m field
000011E0	E5C2D7C5 D9D44040			609+	DC	CL8' VBPERM	instruction name
000011E8	00001250			610+	DC	A(RE3+16)	address of v2 source
000011EC	00001260			611+	DC	A(RE3+32)	address of v3 source
000011F0	00000010			612+	DC	A(16)	result length
000011F4	00001240			613+REA3	DC	A(RE3)	result address
000011F8	00000000 00000000			614+	DS	FD	gap
00001200	00000000 00000000			615+V103	DS	XL16	V1 output
00001208	00000000 00000000						
00001210	00000000 00000000			616+	DS	FD	gap
				617+*			
00001218				618+X3	DS	0F	
00001218	E310 5010 0014		00000010	619+	LGF	R1, V2ADDR	load v2 source
0000121E	E761 0000 0806		00000000	620+	VL	v22, 0(R1)	use v22 to test decoder
00001224	E310 5014 0014		00000014	621+	LGF	R1, V3ADDR	load v3 source
0000122A	E771 0000 0806		00000000	622+	VL	v23, 0(R1)	use v23 to test decoder
00001230	E766 7000 0E85			623+	VBPERM	V22, V22, V23	test instruction (dest is a source)
00001236	E760 9000 080E		00001200	624+	VST	V22, V103	save v1 output
0000123C	07FB			625+	BR	R11	return
00001240				626+RE3	DC	0F	xl16 expected result
00001240				627+	DROP	R5	
00001240	00000000 0000FFFF			628	DC	XL16' 000000000000FFFF 0000000000000000'	result t

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001248	00000000 00000000						
00001250	FFFFFFFF FFFFFFFF			629	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00001258	FFFFFFFF FFFFFFFF						
00001260	00000000 00000000			630	DC	XL16' 0000000000000000 0000000000000000'	v3
00001268	00000000 00000000						
				631			
				632	VRR_C	VBPERM	
00001270				633+	DS	OFD	
00001270		00001270		634+	USING	*, R5	base for test data and test routine
00001270	000012B0			635+T4	DC	A(X4)	address of test routine
00001274	0004			636+	DC	H' 4'	test number
00001276	00			637+	DC	X' 00'	
00001277	00			638+	DC	HL1' 00'	m field
00001278	E5C2D7C5 D9D44040			639+	DC	CL8' VBPERM	instruction name
00001280	000012E8			640+	DC	A(RE4+16)	address of v2 source
00001284	000012F8			641+	DC	A(RE4+32)	address of v3 source
00001288	00000010			642+	DC	A(16)	result length
0000128C	000012D8			643+REA4	DC	A(RE4)	result address
00001290	00000000 00000000			644+	DS	FD	gap
00001298	00000000 00000000			645+V104	DS	XL16	V1 output
000012A0	00000000 00000000						
000012A8	00000000 00000000			646+	DS	FD	gap
				647+*			
000012B0				648+X4	DS	OF	
000012B0	E310 5010 0014		00000010	649+	LGF	R1, V2ADDR	load v2 source
000012B6	E761 0000 0806		00000000	650+	VL	v22, 0(R1)	use v22 to test decoder
000012BC	E310 5014 0014		00000014	651+	LGF	R1, V3ADDR	load v3 source
000012C2	E771 0000 0806		00000000	652+	VL	v23, 0(R1)	use v23 to test decoder
000012C8	E766 7000 0E85			653+	VBPERM	V22, V22, V23	test instruction (dest is a source)
000012CE	E760 5028 080E		00001298	654+	VST	V22, V104	save v1 output
000012D4	07FB			655+	BR	R11	return
000012D8				656+RE4	DC	OF	xl16 expected result
000012D8				657+	DROP	R5	
000012D8	00000000 00000000			658	DC	XL16' 0000000000000000 0000000000000000'	result t
000012E0	00000000 00000000						
000012E8	00010203 04050607			659	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000012F0	08090A0B 0C0D0E0F						
000012F8	FFFFFFFF FFFFFFFF			660	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00001300	FFFFFFFF FFFFFFFF						
				661			
				662	VRR_C	VBPERM	
00001308				663+	DS	OFD	
00001308		00001308		664+	USING	*, R5	base for test data and test routine
00001308	00001348			665+T5	DC	A(X5)	address of test routine
0000130C	0005			666+	DC	H' 5'	test number
0000130E	00			667+	DC	X' 00'	
0000130F	00			668+	DC	HL1' 00'	m field
00001310	E5C2D7C5 D9D44040			669+	DC	CL8' VBPERM	instruction name
00001318	00001380			670+	DC	A(RE5+16)	address of v2 source
0000131C	00001390			671+	DC	A(RE5+32)	address of v3 source
00001320	00000010			672+	DC	A(16)	result length
00001324	00001370			673+REA5	DC	A(RE5)	result address
00001328	00000000 00000000			674+	DS	FD	gap
00001330	00000000 00000000			675+V105	DS	XL16	V1 output
00001338	00000000 00000000						
00001340	00000000 00000000			676+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				677+*			
00001348				678+X5	DS	0F	
00001348	E310 5010 0014		00000010	679+	LGF	R1, V2ADDR	load v2 source
0000134E	E761 0000 0806		00000000	680+	VL	v22, 0(R1)	use v22 to test decoder
00001354	E310 5014 0014		00000014	681+	LGF	R1, V3ADDR	load v3 source
0000135A	E771 0000 0806		00000000	682+	VL	v23, 0(R1)	use v23 to test decoder
00001360	E766 7000 0E85			683+	VBPERM	V22, V22, V23	test instruction (dest is a source)
00001366	E760 5028 080E		00001330	684+	VST	V22, V105	save v1 output
0000136C	07FB			685+	BR	R11	return
00001370				686+RE5	DC	0F	xl16 expected result
00001370				687+	DROP	R5	
00001370	00000000 000000FF			688	DC	XL16' 0000000000000000FF 0000000000000000'	result t
00001378	00000000 00000000						
00001380	FFFFFFFF FFFFFFFF			689	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00001388	FFFFFFFF FFFFFFFF						
00001390	F0E0D0C0 B0A09080			690	DC	XL16' F0E0D0C0B0A09080 7060504030201000'	v3
00001398	70605040 30201000						
				691			
000013A0				692	VRR_C	VBPERM	
000013A0		000013A0		693+	DS	0FD	
000013A0	000013E0			694+	USING	*, R5	base for test data and test routine
000013A4	0006			695+T6	DC	A(X6)	address of test routine
000013A6	00			696+	DC	H' 6'	test number
000013A7	00			697+	DC	X' 00'	
000013A8	E5C2D7C5 D9D44040			698+	DC	HL1' 00'	m field
000013B0	00001418			699+	DC	CL8' VBPERM	instruction name
000013B4	00001428			700+	DC	A(RE6+16)	address of v2 source
000013B8	00000010			701+	DC	A(RE6+32)	address of v3 source
000013BC	00001408			702+	DC	A(16)	result length
000013C0	00000000 00000000			703+REA6	DC	A(RE6)	result address
000013C8	00000000 00000000			704+	DS	FD	gap
000013D0	00000000 00000000			705+V106	DS	XL16	V1 output
000013D8	00000000 00000000			706+	DS	FD	gap
				707+*			
000013E0				708+X6	DS	0F	
000013E0	E310 5010 0014		00000010	709+	LGF	R1, V2ADDR	load v2 source
000013E6	E761 0000 0806		00000000	710+	VL	v22, 0(R1)	use v22 to test decoder
000013EC	E310 5014 0014		00000014	711+	LGF	R1, V3ADDR	load v3 source
000013F2	E771 0000 0806		00000000	712+	VL	v23, 0(R1)	use v23 to test decoder
000013F8	E766 7000 0E85			713+	VBPERM	V22, V22, V23	test instruction (dest is a source)
000013FE	E760 5028 080E		000013C8	714+	VST	V22, V106	save v1 output
00001404	07FB			715+	BR	R11	return
00001408				716+RE6	DC	0F	xl16 expected result
00001408				717+	DROP	R5	
00001408	00000000 000000FF			718	DC	XL16' 0000000000000000FF 0000000000000000'	result t
00001410	00000000 00000000						
00001418	FFFFFFF0 FFFFFFFF00			719	DC	XL16' FFFFFFFF00FFFFFFF00 FFFFFFFF00FFFFFFF'	v2
00001420	FFFFFFF0 FFFFFFFF						
00001428	F0E0D0C0 B0A09080			720	DC	XL16' F0E0D0C0B0A09080 7060504030201000'	v3
00001430	70605040 30201000						
				721			
00001438				722	VRR_C	VBPERM	
00001438		00001438		723+	DS	0FD	
00001438	00001478			724+	USING	*, R5	base for test data and test routine
				725+T7	DC	A(X7)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000143C	0007			726+	DC	H' 7'	test number
0000143E	00			727+	DC	X' 00'	
0000143F	00			728+	DC	HL1' 00'	m field
00001440	E5C2D7C5 D9D44040			729+	DC	CL8' VBPERM	instruction name
00001448	000014B0			730+	DC	A(RE7+16)	address of v2 source
0000144C	000014C0			731+	DC	A(RE7+32)	address of v3 source
00001450	00000010			732+	DC	A(16)	result length
00001454	000014A0			733+REA7	DC	A(RE7)	result address
00001458	00000000 00000000			734+	DS	FD	gap
00001460	00000000 00000000			735+V107	DS	XL16	V1 output
00001468	00000000 00000000						
00001470	00000000 00000000			736+	DS	FD	gap
				737+*			
00001478				738+X7	DS	0F	
00001478	E310 5010 0014		00000010	739+	LGF	R1, V2ADDR	load v2 source
0000147E	E761 0000 0806		00000000	740+	VL	v22, 0(R1)	use v22 to test decoder
00001484	E310 5014 0014		00000014	741+	LGF	R1, V3ADDR	load v3 source
0000148A	E771 0000 0806		00000000	742+	VL	v23, 0(R1)	use v23 to test decoder
00001490	E766 7000 0E85			743+	VBPERM	V22, V22, V23	test instruction (dest is a source)
00001496	E760 5028 080E		00001460	744+	VST	V22, V107	save v1 output
0000149C	07FB			745+	BR	R11	return
000014A0				746+RE7	DC	0F	xl16 expected result
000014A0				747+	DROP	R5	
000014A0	00000000 00000980			748	DC	XL16' 0000000000000980 0000000000000000'	result t
000014A8	00000000 00000000						
000014B0	11223344 55667788			749	DC	XL16' 1122334455667788 99AABBCCDDEEFF00'	v2
000014B8	99AABBCC DDEEFF00						
000014C0	020F1F20 31415161			750	DC	XL16' 020F1F2031415161 718191A1B0B1B2B3'	v3
000014C8	718191A1 B0B1B2B3						
				751			
000014D0				752	VRR_C	VBPERM	
000014D0		000014D0		753+	DS	0FD	
000014D0	00001510			754+	USING	*, R5	base for test data and test routine
000014D4	0008			755+T8	DC	A(X8)	address of test routine
000014D6	00			756+	DC	H' 8'	test number
000014D7	00			757+	DC	X' 00'	
000014D8	E5C2D7C5 D9D44040			758+	DC	HL1' 00'	m field
000014E0	00001548			759+	DC	CL8' VBPERM	instruction name
000014E4	00001558			760+	DC	A(RE8+16)	address of v2 source
000014E8	00000010			761+	DC	A(RE8+32)	address of v3 source
000014EC	00001538			762+	DC	A(16)	result length
000014F0	00000000 00000000			763+REA8	DC	A(RE8)	result address
000014F8	00000000 00000000			764+	DS	FD	gap
00001500	00000000 00000000			765+V108	DS	XL16	V1 output
00001508	00000000 00000000			766+	DS	FD	gap
				767+*			
00001510				768+X8	DS	0F	
00001510	E310 5010 0014		00000010	769+	LGF	R1, V2ADDR	load v2 source
00001516	E761 0000 0806		00000000	770+	VL	v22, 0(R1)	use v22 to test decoder
0000151C	E310 5014 0014		00000014	771+	LGF	R1, V3ADDR	load v3 source
00001522	E771 0000 0806		00000000	772+	VL	v23, 0(R1)	use v23 to test decoder
00001528	E766 7000 0E85			773+	VBPERM	V22, V22, V23	test instruction (dest is a source)
0000152E	E760 5028 080E		000014F8	774+	VST	V22, V108	save v1 output
00001534	07FB			775+	BR	R11	return
00001538				776+RE8	DC	0F	xl16 expected result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001538				777+	DROP R5		
00001538	00000000 0000FF00			778	DC XL16' 000000000000FF00 0000000000000000'	result	t
00001540	00000000 00000000						
00001548	FFFFFFFF FFFFFFFF			779	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2	
00001550	FFFFFFFF FFFFFFFF						
00001558	70605040 30201000			780	DC XL16' 7060504030201000 F0E0D0C0B0A09080'	v3	
00001560	F0E0D0C0 B0A09080						
				781			
				782	VRR_C VBPERM		
00001568				783+	DS OFD		
00001568		00001568		784+	USING *, R5	base for test data and test routine	
00001568	000015A8			785+T9	DC A(X9)	address of test routine	
0000156C	0009			786+	DC H' 9'	test number	
0000156E	00			787+	DC X' 00'		
0000156F	00			788+	DC HL1' 00'	m field	
00001570	E5C2D7C5 D9D44040			789+	DC CL8' VBPERM	instruction name	
00001578	000015E0			790+	DC A(RE9+16)	address of v2 source	
0000157C	000015F0			791+	DC A(RE9+32)	address of v3 source	
00001580	00000010			792+	DC A(16)	result length	
00001584	000015D0			793+REA9	DC A(RE9)	result address	
00001588	00000000 00000000			794+	DS FD	gap	
00001590	00000000 00000000			795+V109	DS XL16	V1 output	
00001598	00000000 00000000						
000015A0	00000000 00000000			796+	DS FD	gap	
				797+*			
000015A8				798+X9	DS OF		
000015A8	E310 5010 0014		00000010	799+	LGF R1, V2ADDR	load v2 source	
000015AE	E761 0000 0806		00000000	800+	VL v22, 0(R1)	use v22 to test decoder	
000015B4	E310 5014 0014		00000014	801+	LGF R1, V3ADDR	load v3 source	
000015BA	E771 0000 0806		00000000	802+	VL v23, 0(R1)	use v23 to test decoder	
000015C0	E766 7000 0E85			803+	VBPERM V22, V22, V23	test instruction (dest is a source)	
000015C6	E760 5028 080E		00001590	804+	VST V22, V109	save v1 output	
000015CC	07FB			805+	BR R11	return	
000015D0				806+RE9	DC OF	xl16 expected result	
000015D0				807+	DROP R5		
000015D0	00000000 0000DB66			808	DC XL16' 000000000000DB66 0000000000000000'	result	t
000015D8	00000000 00000000						
000015E0	FFFFFFFF FFFFFFFF			809	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2	
000015E8	FFFFFFFF FFFFFFFF						
000015F0	0101FF02 02FF0304			810	DC XL16' 0101FF0202FF0304 FF0506FFFF0706FF'	v3	
000015F8	FF0506FF FF0706FF						
				811			
00001600	00000000			812	DC F' 0'	END OF TABLE	
00001604	00000000			813	DC F' 0'		
				814 *			
				815 *	table of pointers to individual load test		
				816 *			
00001608				817 E7TESTS	DS OF		
				818	PTTABLE		
00001608				819+TTABLE	DS OF		
00001608	000010A8			820+	DC A(T1)		
0000160C	00001140			821+	DC A(T2)		
00001610	000011D8			822+	DC A(T3)		
00001614	00001270			823+	DC A(T4)		
00001618	00001308			824+	DC A(T5)		
0000161C	000013A0			825+	DC A(T6)		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001620	00001438			826+	DC	A(T7)	
00001624	000014D0			827+	DC	A(T8)	
00001628	00001568			828+	DC	A(T9)	
				829+*			
0000162C	00000000			830+	DC	A(0)	END OF TABLE
00001630	00000000			831+	DC	A(0)	
				832			
00001634	00000000			833	DC	F' 0'	END OF TABLE
00001638	00000000			834	DC	F' 0'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				836	*****
				837	* Register equates
				838	*****
		00000000	00000001	840 R0	EQU 0
		00000001	00000001	841 R1	EQU 1
		00000002	00000001	842 R2	EQU 2
		00000003	00000001	843 R3	EQU 3
		00000004	00000001	844 R4	EQU 4
		00000005	00000001	845 R5	EQU 5
		00000006	00000001	846 R6	EQU 6
		00000007	00000001	847 R7	EQU 7
		00000008	00000001	848 R8	EQU 8
		00000009	00000001	849 R9	EQU 9
		0000000A	00000001	850 R10	EQU 10
		0000000B	00000001	851 R11	EQU 11
		0000000C	00000001	852 R12	EQU 12
		0000000D	00000001	853 R13	EQU 13
		0000000E	00000001	854 R14	EQU 14
		0000000F	00000001	855 R15	EQU 15
				857	*****
				858	* Register equates
				859	*****
		00000000	00000001	861 V0	EQU 0
		00000001	00000001	862 V1	EQU 1
		00000002	00000001	863 V2	EQU 2
		00000003	00000001	864 V3	EQU 3
		00000004	00000001	865 V4	EQU 4
		00000005	00000001	866 V5	EQU 5
		00000006	00000001	867 V6	EQU 6
		00000007	00000001	868 V7	EQU 7
		00000008	00000001	869 V8	EQU 8
		00000009	00000001	870 V9	EQU 9
		0000000A	00000001	871 V10	EQU 10
		0000000B	00000001	872 V11	EQU 11
		0000000C	00000001	873 V12	EQU 12
		0000000D	00000001	874 V13	EQU 13
		0000000E	00000001	875 V14	EQU 14
		0000000F	00000001	876 V15	EQU 15
		00000010	00000001	877 V16	EQU 16
		00000011	00000001	878 V17	EQU 17
		00000012	00000001	879 V18	EQU 18
		00000013	00000001	880 V19	EQU 19
		00000014	00000001	881 V20	EQU 20
		00000015	00000001	882 V21	EQU 21

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE1	F	00001110	4	566	550	551	553	
RE2	F	000011A8	4	596	580	581	583	
RE3	F	00001240	4	626	610	611	613	
RE4	F	000012D8	4	656	640	641	643	
RE5	F	00001370	4	686	670	671	673	
RE6	F	00001408	4	716	700	701	703	
RE7	F	000014A0	4	746	730	731	733	
RE8	F	00001538	4	776	760	761	763	
RE9	F	000015D0	4	806	790	791	793	
REA1	A	000010C4	4	553				
REA2	A	0000115C	4	583				
REA3	A	000011F4	4	613				
REA4	A	0000128C	4	643				
REA5	A	00001324	4	673				
REA6	A	000013BC	4	703				
REA7	A	00001454	4	733				
REA8	A	000014EC	4	763				
REA9	A	00001584	4	793				
READDR	A	0000001C	4	441	248			
REG2LOW	U	000000DD	1	387				
REG2PATT	U	AABBCCDD	1	386				
RELEN	A	00000018	4	440				
RPTDWSAV	D	00000430	8	312	299	303		
RPTERROR	I	000003DC	4	286	261			
RPTSAVE	F	00000424	4	309	286	306		
RPTSVR5	F	00000428	4	310	287	305		
SKL0001	U	0000004E	1	178	194			
SKL0002	U	00000050	1	206	222			
SKT0001	C	0000022A	20	175	178	195		
SKT0002	C	000002D4	20	203	206	223		
SVOLDPSW	U	00000140	0	114				
T1	A	000010A8	4	545	820			
T2	A	00001140	4	575	821			
T3	A	000011D8	4	605	822			
T4	A	00001270	4	635	823			
T5	A	00001308	4	665	824			
T6	A	000013A0	4	695	825			
T7	A	00001438	4	725	826			
T8	A	000014D0	4	755	827			
T9	A	00001568	4	785	828			
TESTING	F	00001004	4	398	242			
TNUM	H	00000004	2	433	241	289		
TSUB	A	00000000	4	432	245			
TTABLE	F	00001608	4	819				
V0	U	00000000	1	861				
V1	U	00000001	1	862	244			
V10	U	0000000A	1	871				
V11	U	0000000B	1	872				
V12	U	0000000C	1	873				
V13	U	0000000D	1	874				
V14	U	0000000E	1	875				
V15	U	0000000F	1	876				
V16	U	00000010	1	877				
V17	U	00000011	1	878				
V18	U	00000012	1	879				
V19	U	00000013	1	880				

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	5692	0000- 163B	0000- 163B
Regi on		5692	0000- 163B	0000- 163B
CSECT	ZVE7TST	5692	0000- 163B	0000- 163B

STMT	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e7-18-VBPERM asm
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**** NO ERRORS FOUND ****